

In the claims:

1 1. (Original) A method of designing an integrated circuit, comprising:
2 identifying a programmable logic core;
3 identifying an application;
4 designing an application specific circuit for the application; and
5 integrating the programmable logic core into the designed application specific
6 circuit.

1 2. (Previously Presented) A method of designing an integrated circuit, comprising:
2 identifying a programmable logic core for the integrated circuit;
3 establishing a set of timing constraints associated with the programmable
4 logic core; and
5 controlling the design of application specific circuitry that interfaces with the
6 programmable logic core in the integrated circuit in accordance with the set of timing
7 constraints.

1 3. (Previously Presented) A method of designing an integrated circuit, comprising:
2 identifying a programmable logic core for the integrated circuit;
3 establishing a sign-off design associated with the programmable logic core;
4 and
5 controlling the design of application specific circuitry that interfaces with the
6 programmable logic core in the integrated circuit in accordance with the sign-off design.

1 4. (Original) An integrated circuit, comprising;
2 a programmable logic core; and
3 application specific circuitry, the application specific circuitry being designed
4 in accordance with a sign-off design.

1 5. (Previously Presented) An integrated circuit according to claim 4, wherein the
2 programmable logic core includes:
3 a programmable multi-scale array;
4 an application circuit interface for providing a signal interface between the
5 programmable multi-scale array and the application specific circuitry; and
6 a programmable logic core adapter that configures the programmable multi-
7 scale array.

1 6. (Previously Presented) The integrated circuit of claim 5, wherein the
2 programmable multi-scale array comprises an array of configurable arithmetic logic units
3 supporting at least:
4 register transfer level functions; and
5 random logic structures.

1 7. (Previously Presented) The integrated circuit according to claim 4, wherein the
2 programmable logic core comprises a programmable multi-scale array supporting functions
3 of different scales.

1 8. (Previously Presented) The integrated circuit according to claim 4, wherein the
2 programmable logic core includes at a programmable logic core control for loading
3 configuration data into the programmable logic core.

1 9. (Previously Presented) The integrated circuit according to claim 4, wherein the
2 programmable logic core comprises:
3 an array of configurable logic structures having internal storage registers; and
4 a scratchpad memory to supplement the storage registers.

1 10. (Previously Presented) The integrated circuit according to claim 4, wherein the
2 programmable logic core includes at a configuration test interface for data and control flow
3 between the application specific circuit and the programmable logic core.

1 11. (Previously Presented) The integrated circuit according to claim 4 further
2 comprising a microprocessor core communicatively connected to the programmable logic
3 core.

1 12. (Previously Presented) The integrated circuit according to claim 4, wherein the
2 programmable logic core comprises blocks supporting:
3 configuration data control logic;
4 scan path logic; and
5 application circuit interface logic.

1 13. (Previously Presented) The integrated circuit according to claim 4, wherein the
2 programmable logic core comprises arithmetic logic units including:
3 function cells; and
4 an arithmetic logic unit controller.

1 14. (Previously Presented) The integrated circuit according to claim 4, wherein the
2 programmable logic comprises:
3 an internet protocol core; and
4 arithmetic logic units communicatively connected to the internet protocol core.

1 15. (Currently Amended) An integrated circuit, comprising ~~The integrated circuit~~
2 ~~according to claim 4, wherein the programmable logic core supporting:~~
3 a programmable logic core that supports:
4 an idle state that is entered after an assertion of a signal that power is good;
5 a built in self test state for testing the programmable logic core, the built in
6 self test state is entered from the idle state upon receipt of a test
7 command;
8 a configuration state for implementing a configuration process, the
9 configuration state supports entry from the idle state and from the built
10 in self test state after receipt of a configuration clock signal; and
11 an operate state that controls operations of arithmetic logic units, and is
12 entered after completion of the configuration process; and
13 application specific circuitry, the application specific circuitry being designed in
14 accordance with a sign-off design.

1 16. (Previously Presented) An integrated circuit, comprising;
2 means for performing functions associated with a programmable logic core; and
3 means for performing functions associated with application specific circuitry that is
4 designed in accordance with a sign-off design.

- 1 17. (Currently Amended) An integrated circuit, comprising:
- 2 (I) application specific circuitry, the application specific circuitry being designed in
- 3 accordance with a sign-off design; and
- 4 (II) a first programmable logic core including at least
- 5 (A) a programmable multi-scale array having an array of configurable
- 6 arithmetic logic units supporting register transfer level functions, random
- 7 logic structures, and state machine structures,
- 8 (B) an application circuit interface for providing a signal interface between the
- 9 programmable multi-scale array and the application specific circuitry, the
- 10 application circuit interface having test registers for testing the
- 11 programmable logic core,
- 12 (C) scratchpad memories for supplementing storage of the programmable
- 13 multi-scale array,
- 14 (D) a configuration test interface for data and control flow between the
- 15 application specific circuit and the programmable multi-scale array,
- 16 (E) a programmable logic control for loading configuration data into the
- 17 multi-scale array, and
- 18 (F) a programmable logic core adapter that configures the programmable
- 19 multi-scale array through the configuration test interface.

1 18. (Cancelled) A portion of programmable logic program flow comprising:
2 synthesizing data associated with a multi-scalable array and a program logic core
3 design;
4 performing a programmable logic core mapping;
5 performing a programmable logic core placement;
6 performing a programmable logic core routing; and
7 performing a timing and netlist verification.

1 19. (New) The integrated circuit according to claim 15, wherein the first
2 programmable logic core comprises:
3 a programmable multi-scale array comprising a plurality of configurable
4 arithmetic logic units; and
5 a programmable logic core adapter that configures the programmable multi-
6 scale array.

1 20. (New) The integrated circuit according to claim 15, wherein the programmable
2 logic core adapter is configured to receive configuration data and load the configuration data
3 into configuration memory of the programmable logic core adapter.

1 21. (New) The integrated circuit according to claim 15, wherein the first
2 programmable logic core comprises an application circuit interface that interfaces between
3 the programmable multi-scale array and the application specific circuitry.

1 22. (New) The integrated circuit according to claim 15, wherein the programmable
2 multi-scale array performs register transfer level functions.

1 23. (New) The integrated circuit according to claim 15, further comprising a plurality
2 of other programmable logic cores.

1 24. (New) The integrated circuit according to claim 15, wherein the first
2 programmable logic core includes a programmable logic core control for controlling the
3 programmable logic core.

1 25. (New) The integrated circuit according to claim 24, wherein the programmable
2 logic core control provides a control mechanism for testing the first programmable logic
3 core.

1 26. (New) The integrated circuit according to claim 15, further comprising
2 scratchpad memory.

1 27. (New) The integrated circuit according to claim 17, further comprising a
2 configuration data source that stores the configuration data.

1 28. (New) The integrated circuit according to claim 17, further comprising a plurality
2 of other programmable logic cores.

1 29. (New) The integrated circuit according to claim 17, wherein the programmable
2 logic core control provides a control mechanism for testing the first programmable logic
3 core.